The **SAD-1024** is a general-purpose **S**ampled **A**nalog **D**elay device fabricated using N-channel silicon-gate technology in a bucket-brigade configuration to obtain flexible performance at low cost.

KEY FEATURES:

- **Two independent 512-stage delay sections.**
- **Clock-controlled delay: 0.34 sec to less than 340μsec.**
- **N-channel silicon-gate bucket-brigade technology.**
- **Designed for self-cancellation of clocking modulation.**
- **Wide signal-frequency range: 0 to more than 200KHz.**
- **Wide sampling clock frequency range: 1.5KHz to more than 1.5MHz.**
- **Wide dynamic range: S/N > 70db.**
- **Low distortion: less than 1%.**
- **Low noise**
- **Single 15 volt power supply.**

TYPICAL APPLICATIONS:

- **Voice control of tape recorders.**
- **Variable signal control of amplitude or of equalization filters.**
- **Reverberation effects in stereo equipment.**
- **Tremolo, vibrato, or chorus effects in electronic musical instruments.**
- **Variable or fixed delay of analog signals.**
- **Time compression of telephone conversations or other analog signals.**
- **Voice scrambling systems.**

DEVICE DESCRIPTION

The SAD-1024 is a dual 512-stage Bucket-Brigade Device (BBD). Each 512-stage section is independent as to input, output, and clock. The sections may be used independently, may be multiplexed to give an increased effective sample rate, may be connected in series to give increased delay at a fixed sample rate, or may be operated in a differential mode for reduced even-harmonic distortion and reduced clocking noise. Each section has its output split into two channels so that in normal operation output is provided over each full clock period. The SAD-1024 is manufactured using N-channel silicon-gate technology to fabricate a chain of MOS transistors and storage capacitors into a bucket brigade charge-transfer device. It is packaged in a standard 16-lead dual-in-line package with pin configuration as shown in Figure 1. Only V_{dd} and GND are common to the two separate delay sections. Figure 2 shows the functional equivalent circuit diagram. Some of the many applications are listed above.

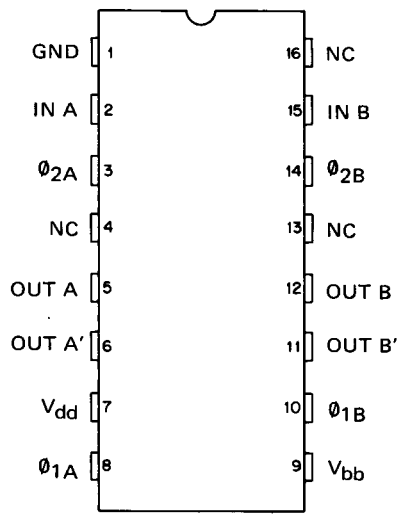

Figure 1. Pin Configuration, SAD-1024. Note: Unused outputs should be connected to V_{dd}; all other unused pins should be connected to GND (pin 1), including those marked N.C.

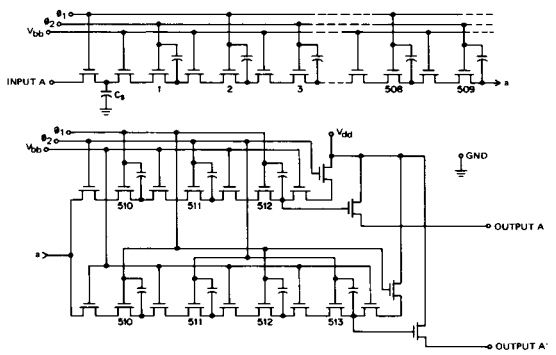

Figure 2. Equivalent Circuit Diagram of either 512-Stage Section of the SAD-1024.

DRIVE AND VOLTAGE REQUIREMENTS

Normal voltage levels and limits are given in the tabular specifications. Clock inputs are two-phase square waves ($Ø_2$ is the complement of $Ø_1$) which swing between ground and V_{dd}. For convenience, V_{bb} may be biased to the same potential as V_{dd}. However, for optimum performance, it is recommended that V_{bb} be adjusted approximately one volt lower than V_{dd}, and that the clock amplitude equal V_{dd}. Unused outputs only should be connected to V_{dd}; other unused terminals (including those marked N.C.) should be connected to ground.

The input analog signal is connected through the first MOS transistor to the input storage capacitor while $Ø_1$ is high; the charge is then transmitted to the next bucket-brigade stage when $Ø_1$ is low, $Ø_2$ high. Thus the signal samples are those values in existence at the positive-to-negative transitions of $Ø_1$ and the input sample rate f_s is the same as $f_{Ø_1}$.

As with all sampled-data devices, the input bandwidth should be limited to a value less than one-half the sampling clock frequency (usually to a value less than 0.3 f_S). Further, to recover a smooth delayed analog output a post filter having steep cutoff (e.g., 36 db per octave) is desirable.

Typical performance of the device is shown in the specifications and in the curves of Figures 4-7. These data were obtained with the test configuration of Figure 3. Internal dispersion becomes the limiting factor for sampling clock frequencies above 1.5MHz.

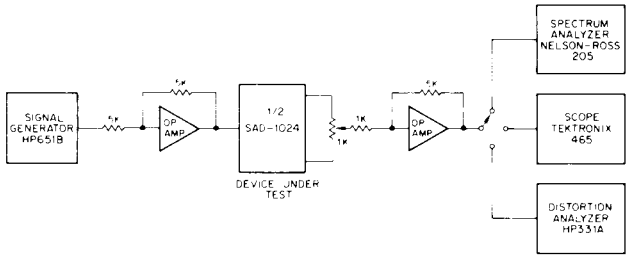

Figure 3. Test Set-up used to obtain the data of Figures 4, 5 and 6.

Figures 4 and 5 indicate the linearity and show the rapid increase in distortion as the input level is increased toward saturation. For inputs less than approximately 500 millivolts rms the distortion is less than one percent. Between this point and the noise floor there is approximately 70 db of dynamic range.

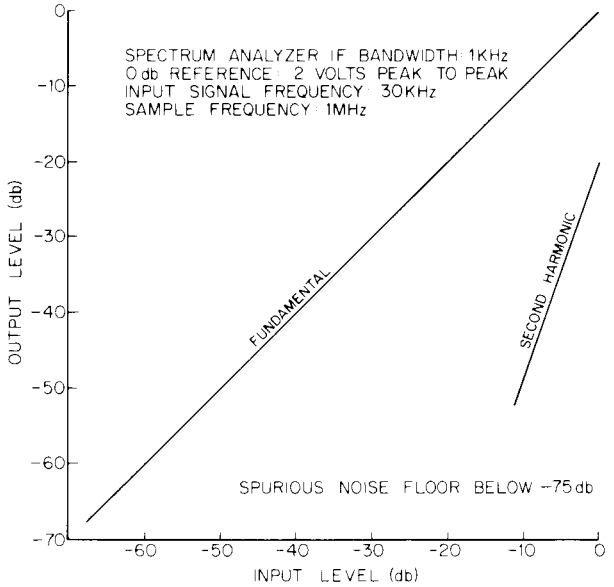

Figure 4. SAD-1024 Transfer Characteristic.

Figure 6 shows the loading effect of the output terminating resistor. The data indicate the output source followers have approximately 400 ohms internal impedance. For this test each output was connected through a terminating resistor to ground, thus isolating any interaction between the two output followers.

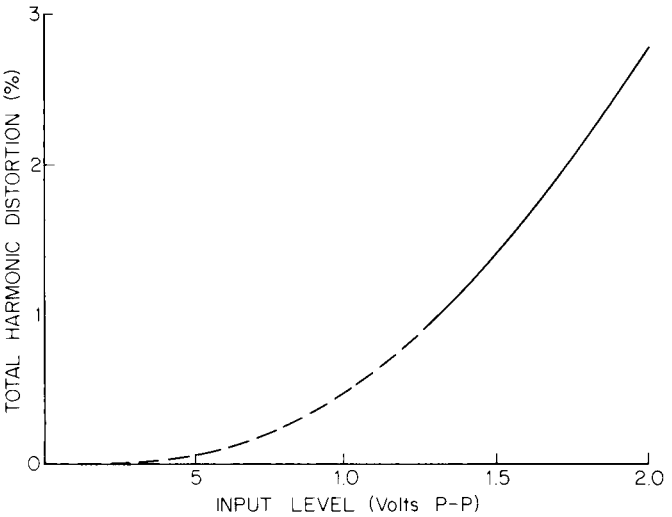

Figure 5. SAD-1024 Distortion vs. Input Level.

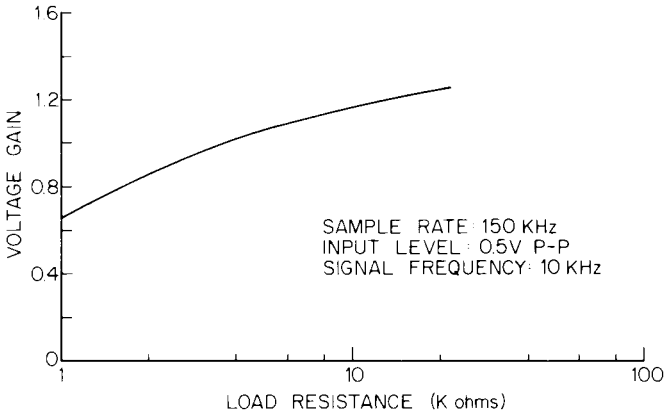

Figure 6. Dependence of Gain on Load Resistance.

Figure 7 shows the frequency response of the device when terminated as shown. The dotted lines indicate the range of variation from device to device.

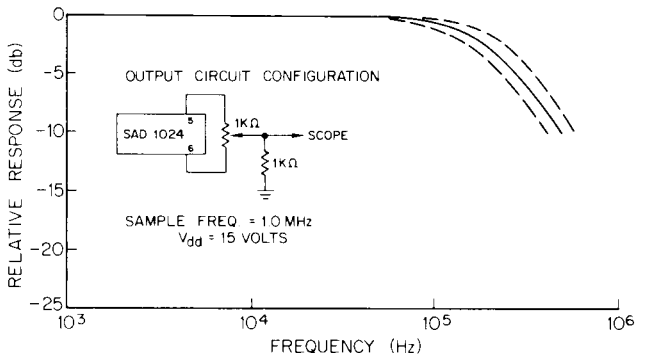

Figure 7. Frequency Response showing Typical Variation Device to Device.

CIRCUIT CONFIGURATIONS

Each SAD-1024 consists of two 512-element delay sections electrically independent except for common grounds and power supplies. The sections may be used in series, in parallel multiplex, in a differential mode, or as completely separate de-

vices. But note that for a given system sample rate, the parallel or differential configuration may be preferable to the series configuration. A number of possible arrangements using one or two devices are described in the following sections.

1. Normal single-section configuration

In this configuration, the A and B sections are independent except for common power-supply connections. Different input signals and different clocks are permissible. A and A′ outputs should be summed externally as in Figure 8. The B and B′ outputs should be similarly summed for the second channel. Delay is 512 clock half periods between the input cutoff at the falling edge of ϕ_{1A} to the end of the output at video A (when ϕ_{1A} likewise falls). Output A′ then appears (with the value previously at Output A) and exists for the next or 513th clock half period. A clock half period is the time duration between successive clock transitions, or one half of a full square-wave cycle. The A section is used for illustration only; the B section performance is completely similar but independent from A.

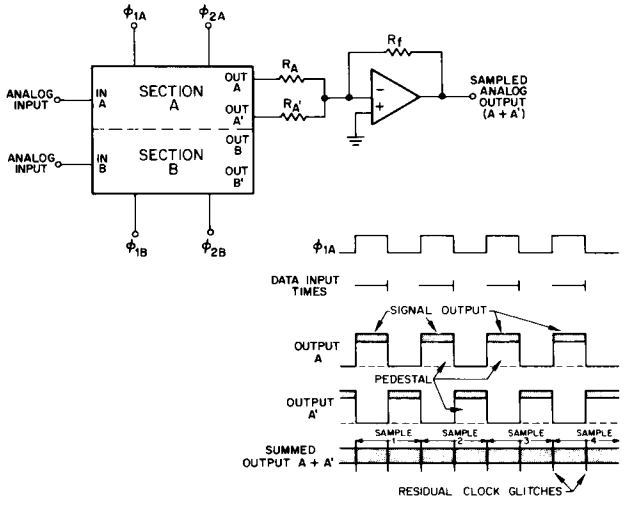

Figure 8. Single-Section Operation. Connect unused outputs to V_{dd} and all other unused pins to ground.

2. Serial configuration

This configuration doubles the permissible delay time for a given sample rate. It is generally preferred when longer delays are required than can be obtained from a single section.

In the serial configuration, output from channel A is slightly attenuated to restore the level to equal that originally input to A, and this modified signal then connected to input B, as in Figure 9. ϕ_{1A} and ϕ_{1B} are connected together as are ϕ_{2A} and ϕ_{2B}. Under these conditions the input to B is that corresponding to output A. Output A′ need not be used except to reduce transients in the output amplifier. It is also possible to obtain 513 clock half-periods of delay from section A by using output A′ to connect to input B and reversing the clocks to B. Unused outputs should be terminated to V_{dd}.

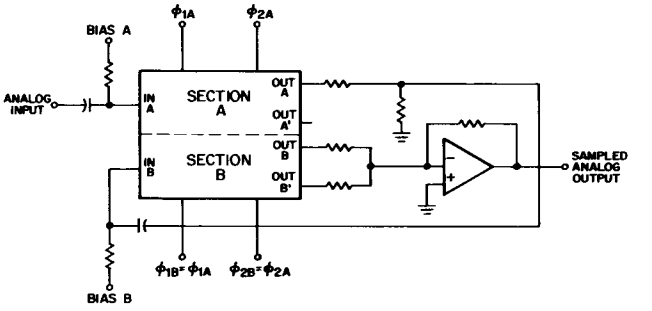

Figure 9. Serial Connection of Delay Sections. Waveforms are entirely similar to those for single-section operation (Figure 8). Connect unused outputs to V_{dd}.

For this configuration note that there is only one sample per clock period, but two clock "glitches" per sample in the output. The Nyquist frequency is $f_N = f_{sample}/2 = f_{clock}/2$.

3. Parallel-multiplex operation

This configuration doubles the number of samples for the same delay or doubles the delay for the same sample rate, when compared to single-section performance. When sample rate is held constant and delay doubled, the individual sections operate at one-half the system rate, so that superior performance is possible. In the parallel multiplex operation, the inputs are paralleled, but the clocks to section B are reversed from those to section A as in Figure 10. Now, on the posi-

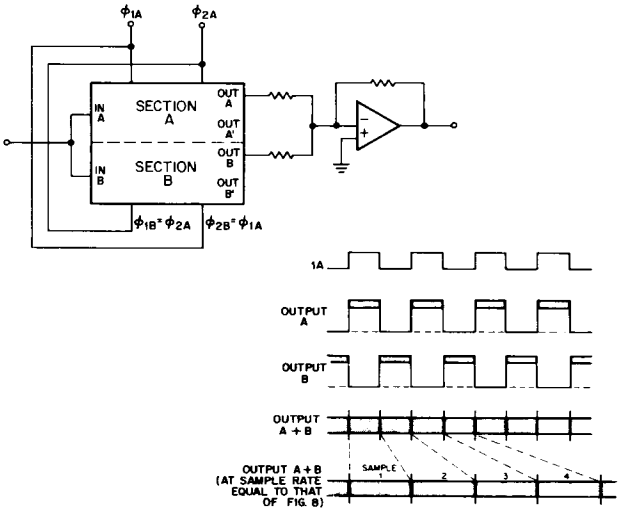

Figure 10. Parallel-Multiplex Operation. Connect unused outputs to V_{dd}.

tive portion of $\emptyset_{1A}$, data is input to section A, to be held and propagated down the bucket brigade at the value present when $\emptyset_{1A}$ falls. Data to section B is input during the positive portion of $\emptyset_{1B}$, which is the same as $\emptyset_{2A}$, so that data is alternately sampled into section A and section B, one sample per half-period of the clock. At the outputs we now sum either outputs A and B (for 512 clock half-periods of delay) or outputs A' and B' (for 513 clock half-periods of delay), but now there are two samples overall per clock period instead of only one. Thus the Nyquist frequency overall is $F_N = f_{sample}/2 = f_{clock}$, or double that for the single section or serial sections operating at the same clock rate. One could thus halve the clock rate to keep the overall sampling rate and Nyquist frequency the same as for the single or serialed sections, but delay is twice that for a single section (equal to that for the serialed sections.) Multiplex operation is generally preferable only when operating at high sample frequencies, as a means of reducing individual section rates. For sample rates of 200 KHz or below, other limitations generally favor serial operation. As before, unused outputs should be connected to V_{dd} and other unused pins grounded.

4. Differential Operation.

In this configuration, more effective cancellation of clocking glitches is possible, because the *same* clock transitions are combined differentially and even-harmonic distortion cancels. The arrangement is as in Figure 11. Operation is similar to that for single-channel operation except for the differential cancellation of the output pedestals and clocking glitches, and cancellation of even harmonics, as in push-pull operation. It should be obvious that two devices could be combined in parallel-multiplex, with each device differentially connected, to give the benefits of a Nyquist frequency equal to the clock frequency, as well as the benefits of differential operation.

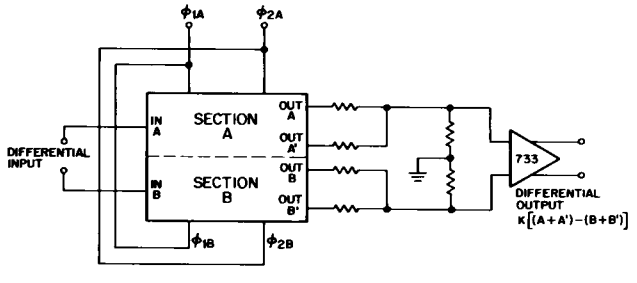

Figure 11. Differential Operation.

5. Multiple-device Operation.

Extension of any of the above methods of operation to multiple devices is possible. Serial operation is restricted by the requirement of gain restoration between sections, by increased dispersion as the number of BBD cells increases, and by all the switching noise of single devices. Note that the SAD-1024 itself exhibits slightly more than unity gain, so that direct serial connection through a resistance network is possible.

Additional units may be multiplexed in the parallel-multiplex configuration by shifting the phase of the clock to successive devices by π/N radians where N is the number of devices. Thus in the case of two devices, for example, device #2 has its clocks shifted by $\pi/2$ radians or 90° from those of device #1.

PERFORMANCE CONSIDERATIONS

The SAD-1024, because of its low cost and clock-fixed delay independent of input frequency, has many applications in the consumer area, particularly for providing delay and its associated effects for audio-frequency devices (e.g., reverberation, vibrato, speed change or correction, etc.). It is very important to remember that the device is a sampled-data device, and as such has important requirements on filtering of the input and output signals and on control of the clock frequency. Also, increased signal amplitude near overload gives rise to rapidly increasing intermodulation products which lie within the useful passband and which thus are not normally reducible by filtering. In the first place, the analog input must be filtered to limit input components to less than $f_{sample}/2$. Normally a stricter limiting is desirable—to a limit more nearly 0.3 f_{sample}. The reason for this requirement is that all input components become modulated by the sampling frequency to generate (f_s-f_{in}) and also many other products. The result is to "fold" the input about $f_s/2$ so that components above $f_s/2$ reappear an equal distance below $f_s/2$. Limiting the input to $f_s/3$ provides a filter "guard band" to permit adequate attenuation of the otherwise disturbing high-frequency components. In the second place, even after combination as indicated, the output is only stepwise continuous, and clocking "glitches" appear at the times of clock transitions. The high frequencies contained in the abrupt changes and in the clocking glitches are all extraneous and for best performance should be removed by a filter with cut-off at approximately $f_{sample}/2$ or less and rolloff of as much as 36 db/octave or more.

For optimized performance, care should be given to layout and design as well as to the filtering requirements. Ground planes are required on circuit boards to reduce crosstalk, and high-quality summing operational amplifiers are required to obtain maximum cancellation of clock pedestals and glitches.

For many applications, however, cost is a more important factor than the ultimate in performance, and relaxed filtering is permissible. However, the user should be well aware of the cost/performance tradeoffs involved. For such relaxed requirements, a simple output circuit such as that shown in Figure 12 is often useful.

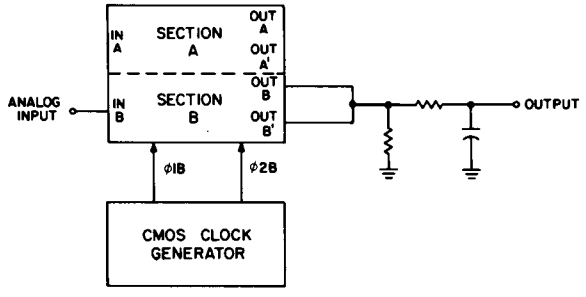

Figure 12a. Simple Output Summing Circuit. Connect unused outputs to V_{dd} and all other unused pins to ground.

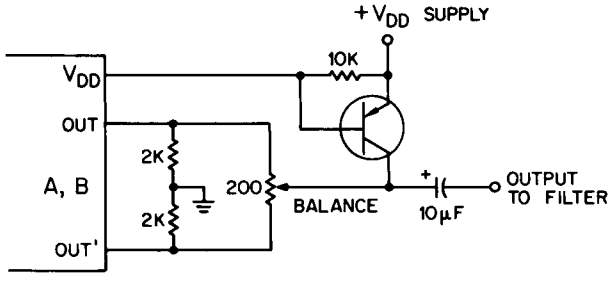

Figure 12b. Feedback Impedance Convert Circuit. Provides improved frequency response and low output impedance. Connect unused outputs to V_{dd} and all other unused pins to ground.

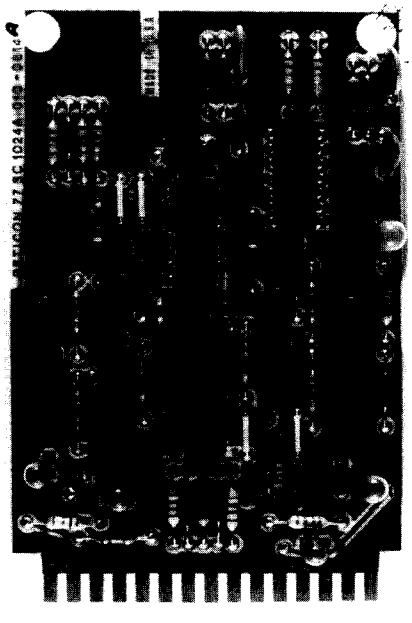

Figure 13. Photograph of SC-1024A Evaluation Board.

EVALUATION CIRCUIT SC-1024 A

For evaluation purposes or for relatively high-performance operation, a circuit board is available from Reticon. This board encompasses the desired filters, clock control, and ground plane. External balanced + and − power supply (nominally ±15 volts) and TTL clock drive is required. Figure 13 is a photograph of the board and Figure 14 is its schematic diagram. Note that the board is arranged such that the two halves of the SAD-1024 may be operated independently, or in series as desired. The separate connection also permits parallel multiplex or differential operation; the series connection is useful for longer delay.

Each output filter amplifier is nominally designed as a two-pole maximally flat filter with cutoff frequency of approximately 20KHz. They follow standard active two-pole filter design, with the source impedance of the SAD-1024 and the balance arrangements taken into account. Change of cutoff frequency requires component changes. For the separate configuration, each section of the SAD-1024 is provided with its own two-pole filter; for the series configuration, the filters are cascaded to improve the out-of-band attenuation. The SAD-1024 provides output from terminal A (or B) during the period $Ø_1$ is high and output from A' (or B') when $Ø_2$ is high. These outputs are summed at the balance potentiometer whose adjustment permits equalization for slight differences in the source-follower outputs from the SAD-1024. The board SC-1024A is designed to handle a wide range of bandwidths and clock rates; as a consequence no attempt has been made to provide band limiting at the input. Anti-aliasing filters should be provided externally if the input is not otherwise limited to a bandwidth less than $f_{sample}/2$.

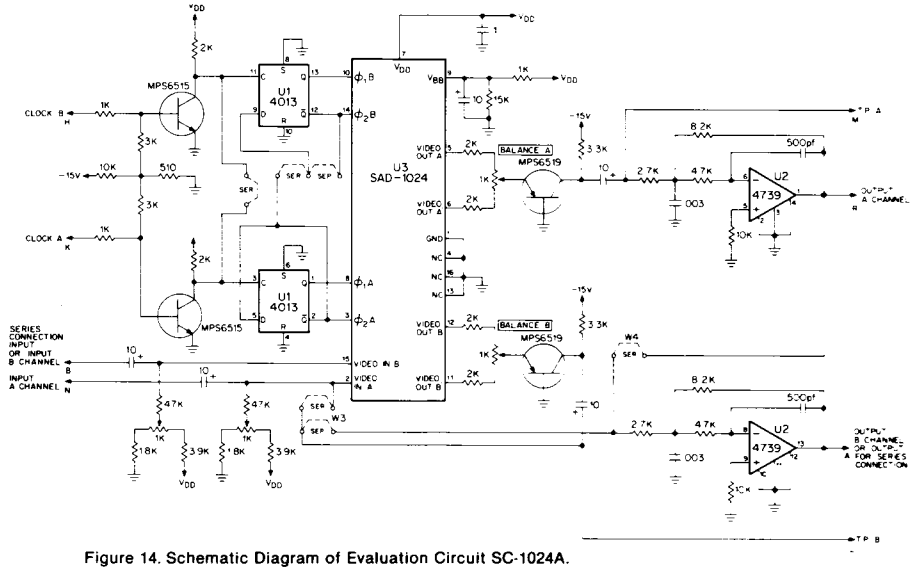

Figure 14. Schematic Diagram of Evaluation Circuit SC-1024A.

DEVICE CHARACTERISTICS AND OPERATING PARAMETERS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock Voltage[1]	$\emptyset_1, \emptyset_2$	10	15	17	Volts
Drain Supply Voltage[1]	V_{dd}	10	15	17	Volts
Bias Voltage[1]	V_{bb}		V_{dd}-1	V_{dd}	Volts
Sampling Freq.	$f\emptyset_1, f\emptyset_2$	0.0015	—	1.5	MHz
Clock Rise Time	t_{cr}		30		nsec
Clock Fall Time	t_{cf}		50		nsec
Clock Line Cap	C_c		110		pf
Signal Freq. Bandwidth (3db point)		See Fig. 7	200		KHz
Signal to Noise		See Fig. 4			
Distortion		See Fig. 5			
Gain[2]			1.2		
Input Capacitance	C_{in}		7		pf
Input Shunt Resistance[3]	R_{in}			200	Kohms
Output Resistance	R_o	See Fig. 6			
Optimum Input Bias[4]			+6		Volts
Maximum Input Signal Amplitude		1	2		Volts p-p
Average Temp. Coefficient of Gain[6]			-.01		db/°C
Average Temp. Coefficient of Optimum Input Bias[6]			.8		mv/°C

ABSOLUTE MAXIMUM VOLTAGES

TERMINAL	LIMITS	UNITS
Any terminal[1]	+20 to -0.4	Volts

Notes:

1. All voltages measured with respect to GND (pin 1).
2. The value of gain depends on the output termination resistance. See Figure 6.
3. Effective a-c shunt resistance measured at 1MHz.
4. The input bias voltage varies slightly with the magnitude of the clock voltage (and V_{dd}) and may be adjusted for optimum linearity at maximum signal level. The value shown is nominal for 15 volt clocks.
5. The device may be operated at clock voltages down to 5 volts (to facilitate use in battery operated portable equipment) but with reduced input bias and reduced input signal amplitude.
6. Measured at sample frequency of 10KHz, audio input of 1V p-p at 1KHz in SC-1024A circuit for temperature range of 0° to 70°C.

WARNING: Observe MOS Handling and Operating Procedures. Maximum rated supply voltages must not be exceeded. Use decoupling networks to suppress power supply turn on/off transients, ripple and switching transients. Do not apply independently powered or AC coupled signals or clocks to the chip with power off as this will forward bias the substrate. Damage may result if external protection precautions are not taken.

SAD-512 SINGLE 512-STAGE ANALOG DELAY LINE

The SAD-512 is identical to one 512-stage section of the SAD-1024; all of the specifications and characteristics of the latter device apply equally to the SAD-512. Figure 15 shows the pin configuration of the SAD-512. Note that pin assignments are identical to those for the A section of the SAD-1024. In some instances, SAD-1024 devices having an inoperative B section may be used to make SAD-512 devices. It is, therefore, essential that unused pins 10, 14, and 15 be connected to ground, and that pins 11 and 12 be connected to V_{dd}.

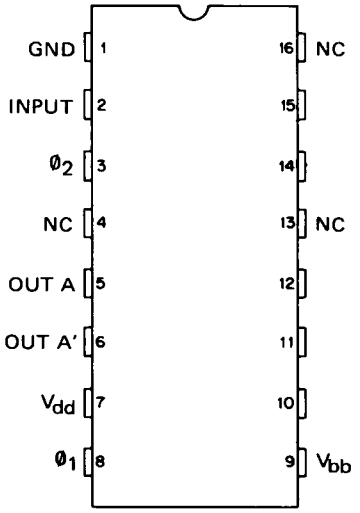

Figure 15. Pin Configuration, SAD-512.

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